UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

Ultra High Step-Up DC-DC Converter Fuzzy Controller using Three Degree of Freedom Approach (3DoF)

R. Naveen Kumar[1], G. Ramesh[2]

M. Tech Dept of EEE, Vignan Lara Institute of Technology and Science, Guntur, India[1]

Assistant Professor, Dept of EEE, Vignan Lara institute of Technology and Science, Guntur, India[2]

Abstract: A novel ultrahigh step-up dc–dc converter, which utilizes the features of modularity, multilevel and electrical isolation is proposed in this paper. To achieve an ultrahigh step-up ratio a novel dc–dc converter topology while maintaining a high conversion efficiency. It adopts a three degree of freedom approach in the circuit design. New control strategies including the two-section output voltage control and cell idle control are also developed to improve the converter performance. To a wide range of high voltage and high power distributed generation and dc power transmission the step-up conversion ratio can reach 1:14 with a peak efficiency of 94% and the proposed techniques can be applied. By using the simulation results we can analyse the proposed method. To improve the performance, a novel control strategy using Fuzzy Logic Controller (FLC) is proposed it will eliminates the drawback of using fixed gain in conventional PI controller.

Index Terms: Boost converter, control strategy, dc–dc power conversion, degrees of freedom (DoF), high step-up converter, and modularization.

I. INTRODUCTION

Distributed generation is plays an important role in reducing green house gas emissions and improving quality of human lives. In these systems, power converters are plays a major role to control the power flow in a system. In particular, solar power generation, fuel cells, electrical vehicles, and uninterrupted power supplies are used high step-up DC-DC converters. [1]-[13]. And also the features of DC-DC conversion are essential to off-shore wind power transmission through high voltage dc (HVDC) power systems [14]-[15]. In DC-DC converter applications, high voltage gain and high conversion efficiency are highly desirable.

A high voltage gain is traditionally achieved by to control the transformer's turn's ratio, the pulse width modulation duty ratio or phase-angle. The duty ratio of high frequency switching devices is often consider as one design freedom while the turns ratio of transformer is another [16]-[28]. When both are employed to achieve a high voltage conversion ratio then it is termed as Two Degree of Freedom (2DoF) deign [17],[21],[23]. When an active or passive clamping circuit is implement by using soft switching feature. An active clamping circuit is having the one switching device and one clamping capacitor. Passive clamping circuit uses the switching devices (ex. Diodes) for the required purpose. Generally, the leakage inductance is proportional to square root of the turns ratio. As a result a very high turns ratio is generally avoid in the transformer design. It can reduce the efficiency of the transformer. The high step-up converters uses only one switching devices while the converters ratings is low. Due to the size of converters, the power density of these converters decreases as a voltage gain increases. In literature, some high step-up converters ratios are also reported by combining the features of turns ratio. The input-parallel output-series structure can also provide a high voltage gain and a high power level. coupled inductors are used to achieve a high voltage gain but electrical isolation is absent. Alternatively cascaded converter structure can provide a high voltage gain. The high voltage gain is limited in converters power ratings due to high current in switching devices. To increase the order of power level, a modular multilevel converter is presented. But the modular multilevel converter can regulate only duty ratio and cell number (i.e.2DoF). These topologies are not provided electrical isolation, and sufficient flexibility for the further expansion.

The voltage gain of two degree of freedom converter is

$$G = (2\ N) / (1 - D) \quad \text{---------- (1)}$$

Where N –Turns ratio

D-duty ratio

A small change in the duty ratio can lead to a change in the voltage gain. Then the converter control is difficult then the output voltage regulation is difficult. So to reduce these problems, this paper proposes the ultra high step-up DC-DC

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

converter, because it utilizes the features of modularity, electrical isolation. This is called **Three Degree of Freedom design (3DoF**) of DC-DC converter.

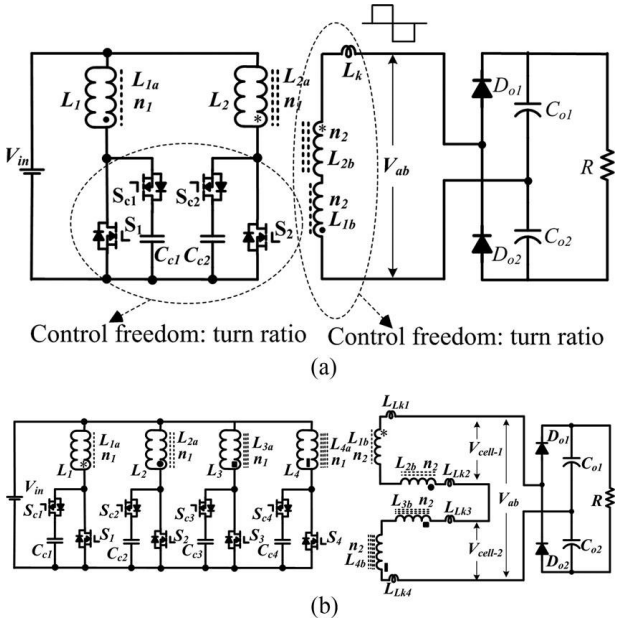


Fig 1. DC–DC converter topologies with fly back-forward cells. (a) Typical fly back-forward converter (b) Proposed fly back-forward dc–dc converter (using two cells).

II. PROPOSED 3DoF CONVERTER TOPOLOGY

Based on the topology we alternatively placed fly-back forward DC-DC converter which is presented in Fig 1(b). The voltage gain can be given by

$$G = (V\ out) / (V\ in);$$

$$= \frac{2N}{(1-D)} \cdot \frac{1}{1+\sqrt{\frac{(2Llk\ .fs)}{(1-D)\hat{}2.R}}} \quad \text{---------- (2)}$$

Where Llk is the leakage inductance,

Fs is the switching frequency and

R is the resistance. Clearly, the voltage gain is determined by the leakage inductance of the coupled inductor, switching frequency, load resistance, in additional turns ratio and duty ratio.

If the secondary side of the fly back forward DC-DC converter is seen as cell, more cells can be added up in series, as shown in fig1(b). by doing so, a multilevel output voltage can be obtained. The corresponding voltage gain in an idea condition is given by

$$G = \frac{2m.N}{1-D} \quad \text{----------} \quad (3)$$

Where m denotes the number of voltage levels. This paper develops a two-cell high step-up dc–dc converter as an example and its topology is shown in Fig. 1(b), where S1–S4 are four main switches. Active clamping circuits including clamp switchesSc1−Sc4and clamping capacitorsCc1−Cc4 are employed to limit the voltage stress on the main switches.

Four coupled inductorsL1–L4are used to form two power cells (L1 andL2 for cell-1, L3 andL4 for cell-2). The primary and secondary winding turns for the four coupled inductors are represented byn1 andn2, respectively, and their turns ratio is N= n2/n1. The coupling references are remarked with "∗", "O", "" and "".LLK1−LLK4are the leakage inductances for coupled inductorsL1−L4, respectively. In this figure, the rectifier diodesDo1−Do2 and the output capacitorsC1–C2 also form a voltage-doubling rectifier circuit.

The proposed converter is built on basic cells; each of them consists of two coupled inductors and a power switch. Typical steady-state waveforms of this converter are shown in Fig. 2. The active clamping switchesSC1−SC4 are complementary to the main switchesS1–S4, respectively. The outputs of cell-1 and cell-2 areVcell−1 andVcell−2, respectively.

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

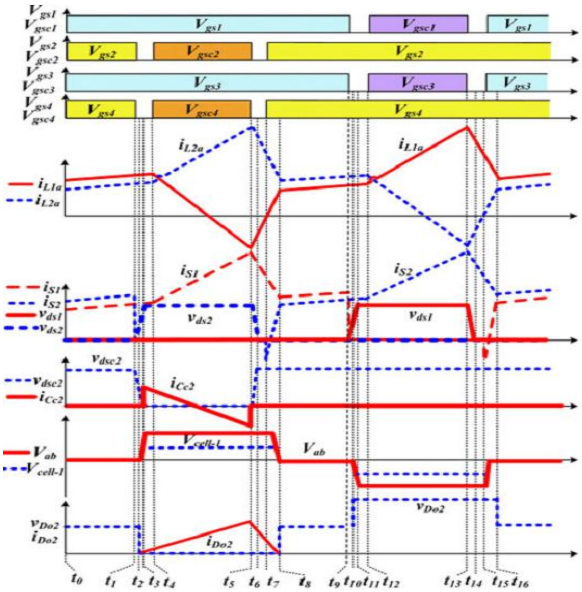
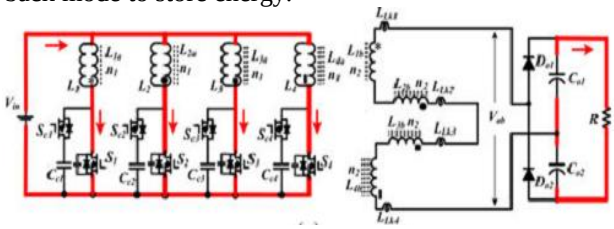


Fig. 2. Waveforms of the proposed converter.

The switches S1–S4 can be regulated by earthier duty ratio control or phase angle shift control. The waveforms ofVcell−1andVcell−2are identical. The proposed converter has eight operational stages, as shown in Fig. 3.

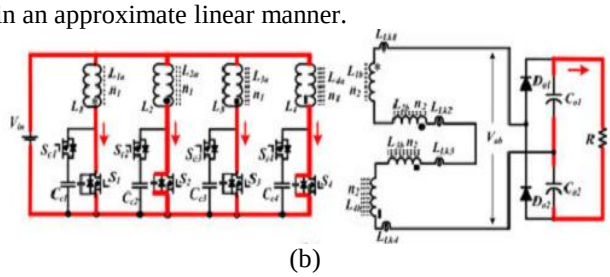
State 1[t0–t1]: During this stage,S1~S4are turned on and the corresponding clamping switches are OFF. All the coupled inductors operate in flyback mode to store energy.



(a)

The outputs of cell-1 and cell-2 are zero and the output rectifier diodes are both reverse-biased. The output capacitorsC01 andC02 supply the energy to the load.

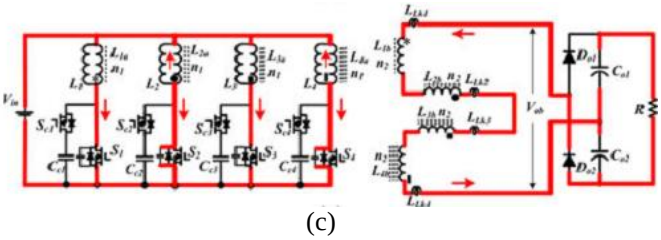
State 2[t1–t2]:Att1, S2 andS4 receive a turn-off gate signal, increasing their drain–source voltage across the parasitic capacitor of the main switches in an approximate linear manner.



(b)

Due to the low parasitic capacitance and the large current in the primary coupled inductor, this period is very short.

State 3[t2–t3]: Att2, the drain–source voltage of S2 andS4 increases to conduct the output rectifier diodes Do2.During this interval,L1(in cell-1) andL3(in cell-2) operate in forward mode whileL2 andL4 in a flyback mode to transfer energy to the load.



(c)

UGC Approved Journal

IARJSET

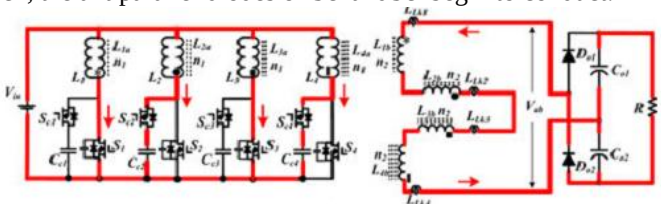
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

State 4[t3–t4]: In this stage, the voltage across the parasitic capacitor ofS2andS4increases to the corresponding voltage of clamp capacitorsCc2 andCc4, the antiparallel diodes of Sc2andSc4begin to conduct.

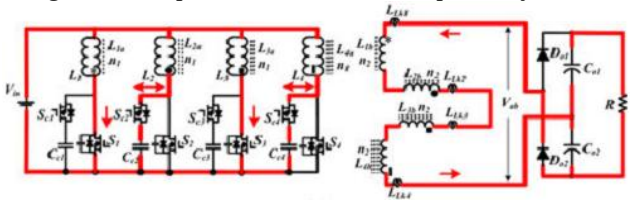


(d)

State 5[t4–t5]: Att4, Sc2 andSc4 are switched on with zero voltage switching (ZVS). Then, a current flows in the anti parallel diode. During this interval, cell-1 and cell-2 provide a continuous current to the load, i.e.,

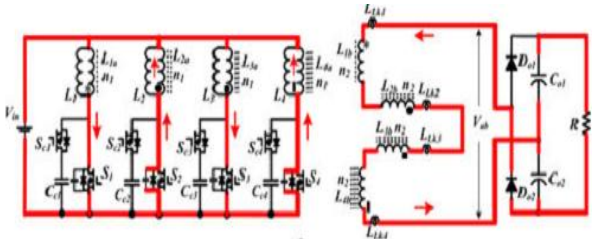
$$i_{LK1}(t) = \frac{N.V_{Cc2} + N.V_{Cc4} - V_{Co1}}{L_{LK1} + L_{LK2} + L_{LK3} + L_{LK4}} . (t - t_4) \qquad (4)$$

whereVCc2 andVCc4 are the voltage across capacitorsCc2 andCc4, respectively.



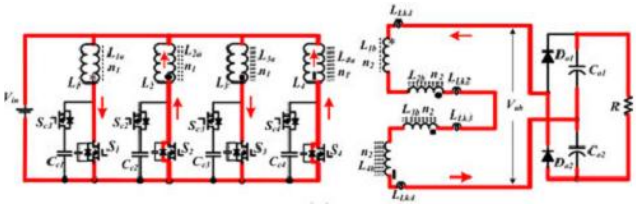
(e)

State 6[t5–t6]: Att5, Sc2 andSc4 receive a turn-off signal. Because of the parallel capacitorsCs2 andCs4, the voltage acrossS2andS4decreases in an approximately linear manner and that inSc2 andSc4 increases nearly linearly. Over this period,Sc2andSc4are turned off with ZVS.



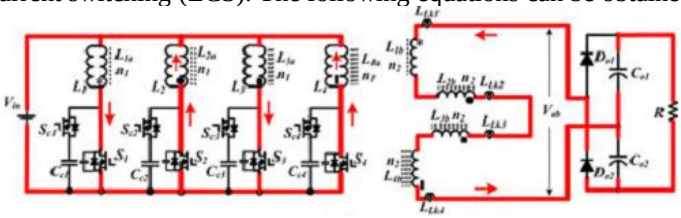
(f)

State 7[t6–t7]: Att6, the drain–source voltage of S2 andS4 decrease to zero owing to the capacitor-inductance resonant. Then, the corresponding anti parallel diode conducts.



(g)

State 8[t7–t8]: Att7, S2 andS4 turn on with ZVS. The leakage currents of cell-1 and cell-2 decrease to zero andD02turns off with zero-current switching (ZCS). The following equations can be obtained:



(h)

Fig. 3. Eight operational stages of the proposed converter (using two cells).(a) State 1[t0−t1]. (b) State 2[t1−t2]. (c) State 3[t2−t3]. (d) State 4[t3−t4]. (e) State 5[t4−t5]. (f) State 6[t5−t6]. (g) State 7[t6−t7]. (h) State 8[t7−t8].

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

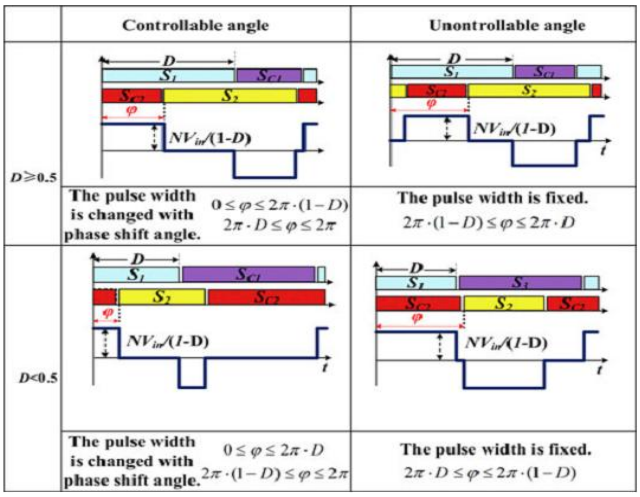


Fig. 4. Phase-angle shift control.

III. STEADY-STATEANALYSIS

In order to simplify the analysis of the proposed converter, the following assumptions are made:
1) all the four coupled inductors are identical;
2) all the clamping capacitors are identical;
3) the voltage of the clamping capacitors is constant;
4) the dead-time between the main switches and clamping switches is neglected.

A. Voltage Stress

The voltage stress on switching devices is equal to the voltage across the clamping capacitors

$$V_{DSi} = V_{Cci} = \frac{V_{in}}{1-D} \quad (5)$$

Where VCc iis the voltage of the active clamping switch, VDSi is the voltage of the main switch, and Vin is the input voltage. According to the symmetrical waveforms of Vab, the voltage stress on the output diodes can be found by

$$V_{co1} = V_{co2} = V_{out} \quad (6)$$

B. Voltage Gain

However, the leakage inductance of the coupled inductor can also impact on the voltage gain. In a two-level high step-up converter, the electrical charge ofCo1 is half of the total electrical charge due to the symmetry of the rectifier circuit

$$Q_{Co1} = \frac{1}{2}.\frac{V_{out}}{R}.T_s \quad (7)$$

C. Soft Switching

Soft switching of power devices can reduce the switching power loss and thus improve the energy efficiency of the converter. In order to realize ZVS for the clamp switches, the antiparallel diodes of clamp switches should conduct prior to the turn-on of the switches. For the main switches, the energy stored in parasitic capacitors should be lower than that stored in the leakage inductor. The ZVS turn-on condition for the main switches is

$$\frac{1}{2}\frac{L_{LKi}}{N_i^2}I_i^2 \geq \frac{1}{2}C_{DSi}V_{DSi}^2 \quad (8)$$

Where Ii is the primary input current of the power step-up cell and CDSi is the parasitic capacitor voltage.

IV. CONTROLSTRATEGIES FOR THEPROPOSEDCONVERTER

There are two control strategies developed to control the output voltage of the proposed converter: the two-section output voltage control and the module idle control.

A. Two-Section Output Voltage Control

In the proposed converter, the output voltage is built up by connecting several voltage sources in series, similar to Fig. 1(b). Therefore, the total voltage gain is the sum of individual cells. The output voltage ofmcells includes two parts: the output voltage ofm–1 cells, and power cellm(used for minor adjustment of the output voltage to limit the duty ratio

UGC Approved Journal

IARJSET

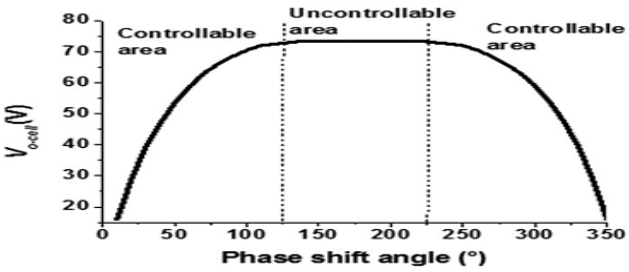
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

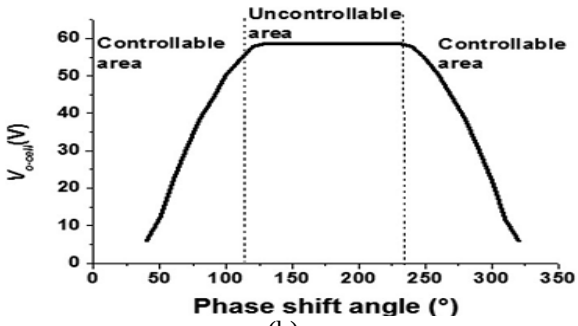
ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

change). Moreover, the phase-angle shift with respect to the turn-on signal ofS1 (see Fig. 2) can be employed to adjust the output voltage of each cell. This has two conditions: controllable and uncontrollable, as illustrated in Fig. 4. The output voltage control underD0.5 andD<0.5 is further presented in Fig. 5.



(a)



(b)

Fig. 5. Output voltage with the phase-angle shift control. (a) 0.66 duty ratio.(b) 0.33 duty ratio

At a shift angle of 180°, the output voltage peaks. In the power cell the two main switches are usually of 180°shift angle, which is in an uncontrollable range, as shown in Figs. 4 and 5. When all cells use the same duty ratio, the phase-angle shift can be employed to control the converter output voltage.

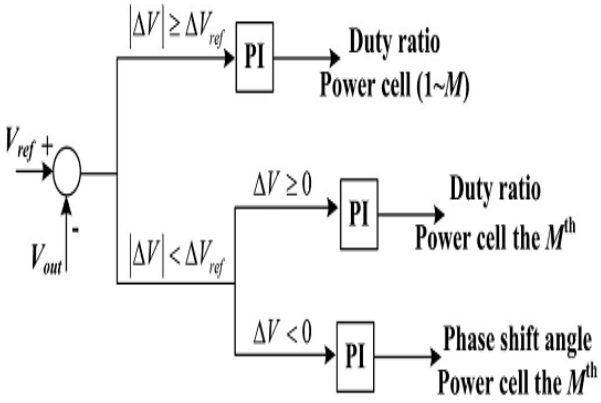


Fig. 6. Schematic diagram of the proposed control strategy.

Fig. 6 illustrates the proposed converter control strategy. ΔVref is the threshold value of voltage error. For a given voltage error, major and minor adjustments can be decided.

B. Cell Idle Control

In the proposed topology, power cell idle conditions can be employed to adjust the voltage gain. If the primary main switching devices are idle, the secondary winding inductor changes from an alternating square voltage source to an inductor. Since the secondary windings of the coupled inductor are series connected; the winding inductance of the idle power cell blocks the current, which is generated from other cells. In this paper, a shielding control strategy is developed for idle power cells by controlling the coupled inductor output with reverse polarity. It is needed to send a turn-off signal to the main switching devices and a turn-on signal to the idle power cells, as presented in Fig. 7

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

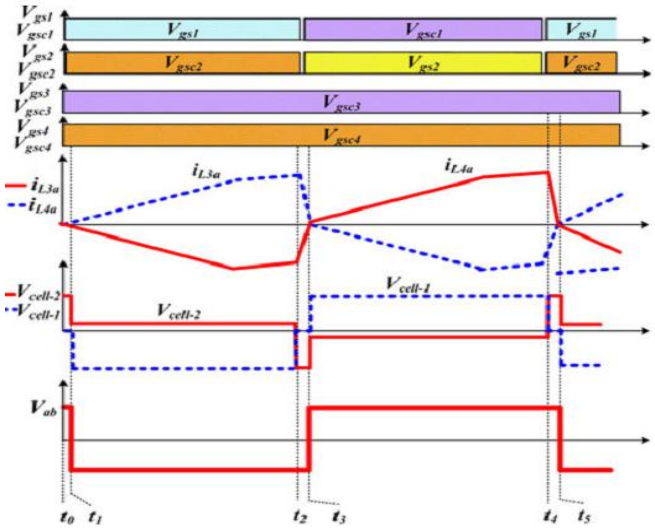


Fig. 7. Waveforms of the shielding control under modular power cell idle conditions.

The output of Vcell−2 is zero during [t1–t2]and[t3– t4] that ensures the energy flow from Vcell−1 to the load. The equivalent circuit of the idle power cell is shown in Fig. 8.

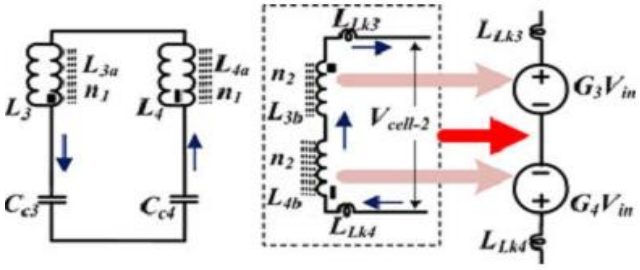


Fig. 8. Equivalent circuit of the idle modular power cell.

Both L3andL4operate in flyback mode, and the secondary side voltage sources are effectively reverse connected. At this condition, the secondary inductor of the idle module is bypassed. In the idle cells, the power losses (associated with the wire resistance and on-state conducting loss of clamp switches) are very low. In effect, cell-1 can operate at the rated output power so as to improve the converter efficiency. In order to study the mechanism of the cell idle mode, the PSIM simulation software is employed to model the converter.

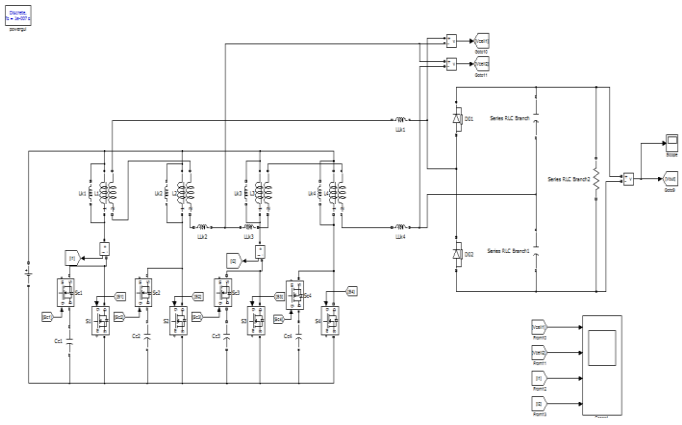


Fig.9.Block diagram of simulation

In Fig. 10, a two-cell topology is used as an example. The input voltage is 15 V and the turn ratio is 2. One cell is idle and the other cell is operational. The output voltage of the operating cell is 60 V while the peak output voltage of the idle cell is 3 V, which is associated with the leakage inductance.

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

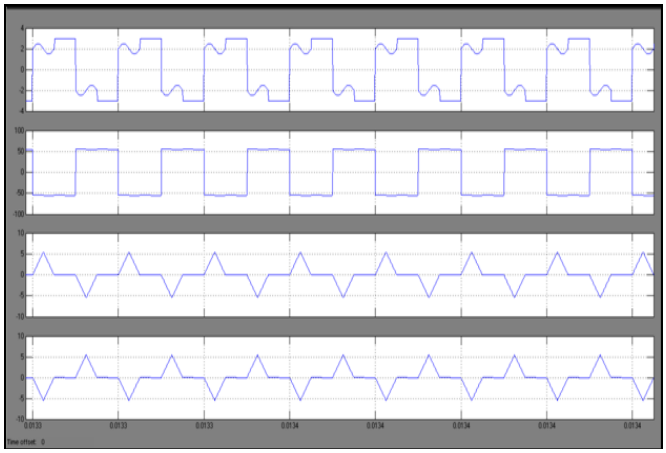


Fig. 10. Simulation results for the cell idle control.

V.FUZZY LOGIC CONTROLLER

FLC is one of the most successful operations of fuzzy set theory. Its chief aspects are the exploitation of linguistic variables rather than numerical variables. FL control technique relies on human potential to figure out the systems behavior and is constructed on quality control rules.. The basic structure of an FLC is represented in Fig.11.

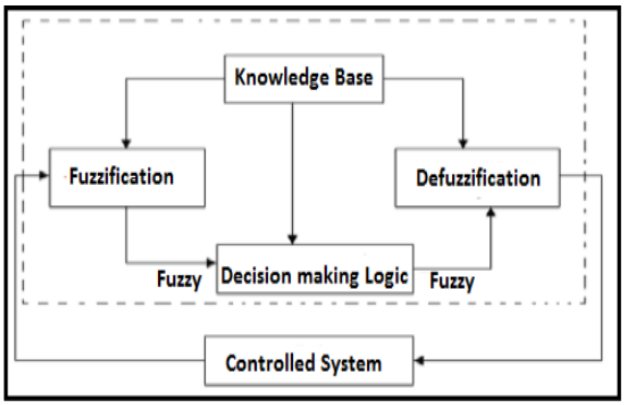


Fig.11. Basic structure of Fuzzy Logic controller

• A Fuzzification interface alters input data into suitable linguistic values.
• A Knowledge Base which comprises of a data base along with the essential linguistic definitions and control rule set.
• A Decision Making Logic which collects the fuzzy control action from the information of the control rules and the linguistic variable descriptions
• A Defuzzification interface which surrenders a non fuzzy control action from an inferred fuzzy control action. In this paper, an advanced control strategy, FLC is implemented along with UPQC for voltage correction through Series APF and for current regulation through Shunt APF. Error and Change in Error are the inputs and Duty cycle is the output to the Fuzzy Logic Controller as shown in Fig. 12-Fig.14

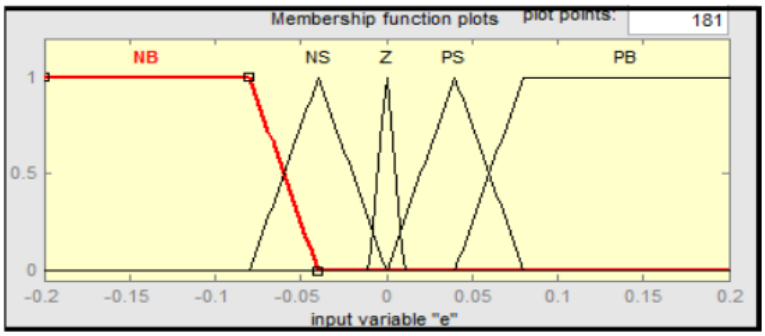


Fig.12. Error as input

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

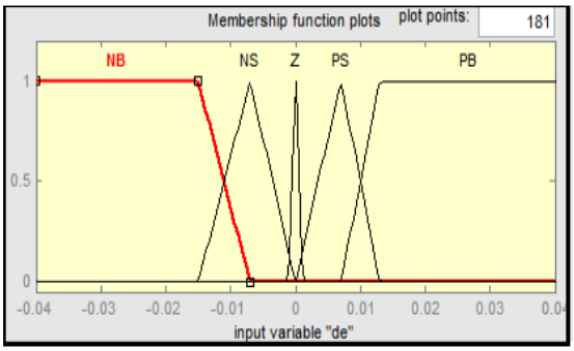


Fig.13 Change in Error as input

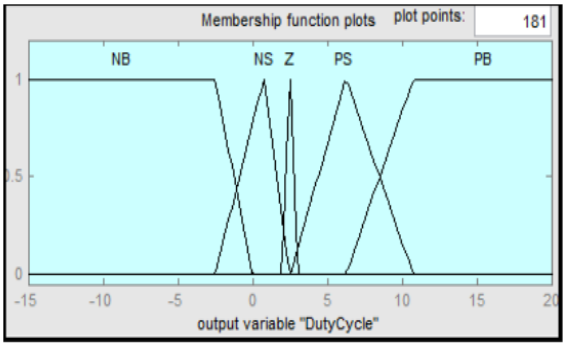


Fig.14 Output variables to defuzzification process

VI. EXPANDABLECHARACTERISTIC AND PERFORMANCECOMPARISON

The proposed 3DoF topology is flexible and expandable. First, it can combine with the interleaved structure to expand the power level, as shown in Fig. 11

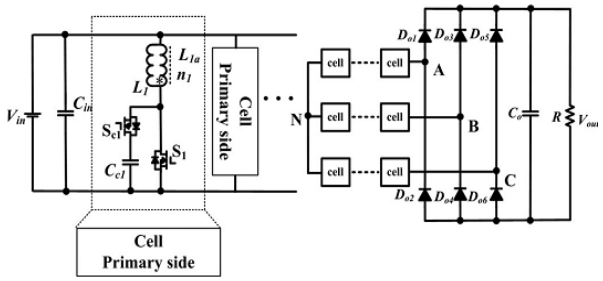
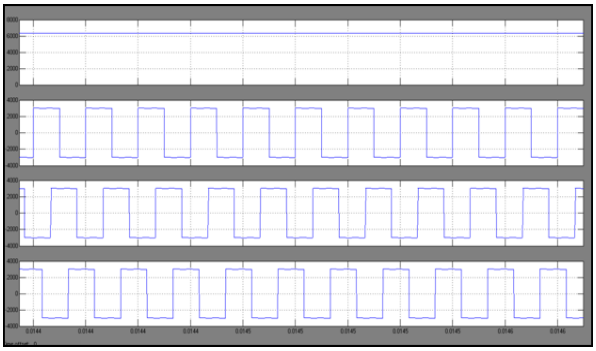


Fig. 11. Three DoF converter with the interleaved structure.

Furthermore, with the development of high voltage silicon carbine (SiC) devices [46], the topology can be applied to HVDC power transmission for offshore wind power. In the simulation, the input voltage is 100 V, converter power is 100 kW, switching frequency is 50 kHz, each winding arm has four cells. Simulation results are shown in Fig. 12.



(a)

UGC Approved Journal

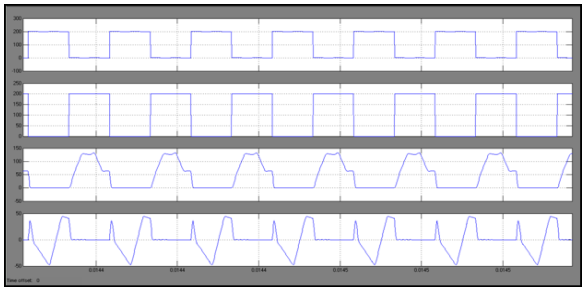
IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017



(b)

Fig. 12. Simulation results for the 3DoF with the interleaved structure. (a) Output voltage and winding arm output. (b) Voltage and current of the primary switching devices.

The structure cannot be used to achieve a high power output. In this paper, a new solution is to combine with the input-parallel output-series structure, as shown in Fig. 13.

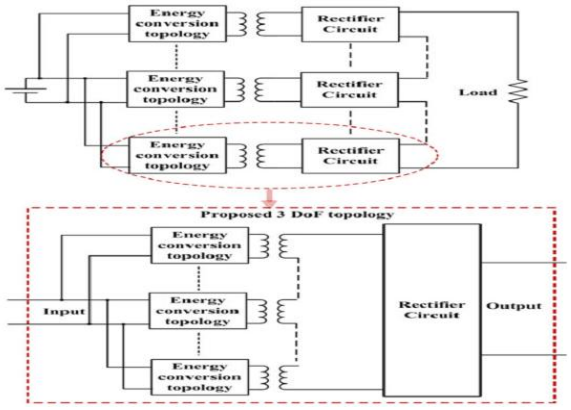


Fig. 13. Three DoF converter with the input-parallel output-series structure.

In this case, the 3DoF topology can be seen as a cell in the traditional input-parallel output-series topology to build up a high-voltage gain converter. The secondary diodes can be achieved by connecting low- voltage diodes in series and parallel connections. Therefore, by introducing a new design freedom, the proposed topology can incorporate features of traditional input-parallel output-series converters to increase voltage (via series-connection) and power (via parallel-connection) to meet the requirements. Based on the previous analysis, a performance comparison of different dc–dc converter topologies is presented in Table I. The features of interleaved structure and input-parallel output series structure can be used in the proposed 3DoF to increase both power and voltage, as shown in Fig. 14.

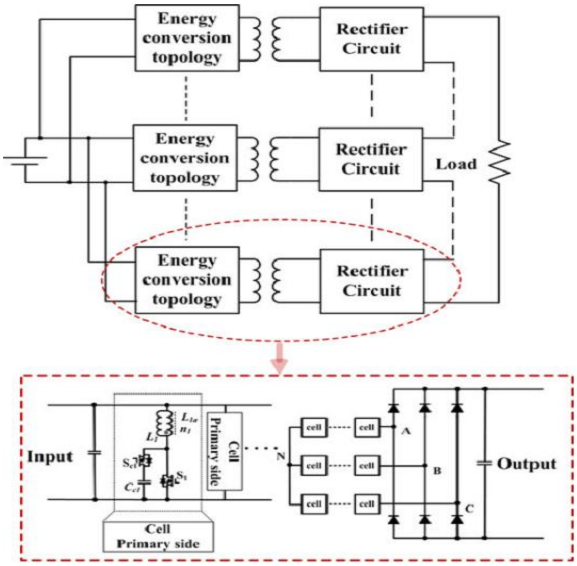


Fig. 14. Proposed 3DoF converter for high power and high voltage-gain output.

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

The single cell efficiency, one-cell-operating one-cell-idle efficiency and overall converter efficiency are calculated and presented in Fig. 15. In the power cell idle condition, due to the parasitic resistance in the primary side capacitors and inductors and secondary winding resistance of the idle cell, the converter efficiency is lower than that for a single cell working condition, but is higher than the two-cell operating condition. By using power cells in an idle mode, the converter can maintain a relatively high efficiency over a wide output power range.

TABLE I PERFORMANCECOMPARISON

Topology	Converter in [42]	Converter in [47]	Converter in [48]	Proposed converter
Modular structure	No	Yes	No	Yes
Power density	Medium	Low	Medium	High
Stressed devices	No	Transformer	Main switching devices	Secondary-side diode
Switching devices voltage stress	$\frac{V_{in}}{1-D}$	Depending on cell voltage	$\frac{2}{1-D}V_{in}$	$\frac{V_{in}}{1-D}$
Expandability	No	Yes	No	Yes
Soft switching	Yes	No	No	Yes
Electrical isolation	No	Yes	No	Yes
Power rating	Low	High	Low	High

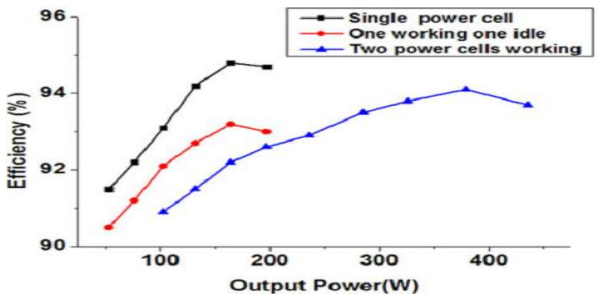


Fig. 15. Measured efficiency of the proposed converter at different conditions.

TABLE II SPECIFICATIONS OF THE PROPOSED CONVERTER

Component/Parameter	Value
Power level (P_{out})	400 W
Input voltage (V_{in})	5~ 10 V
Load resistance (R)	44 Ω
Output voltage (V_{out})	50~ 100 V
Switching frequency (f_s)	50 kHz
Main switches ($S_1 \sim S_4$)	FDP047AN
Clamp switches ($S_{c1} \sim S_{c4}$)	FDP047AN
Rectifier diodes (D_{o1}, D_{o2})	FEP30DP
Clamp capacitors ($C_{c1} \sim C_{c4}$)	4.7 μF
Output capacitor (C_{o1} and C_{o2})	470 μF
Turns ratio ($N = n_2/n_1$)	40:10

TABLE III SPECIFICATIONS OF THE COUPLED INDUCTORS

	Primary inductance	Primary leakage inductance	Secondary inductance	Secondary leakage inductance
L_1	28.65 μH	1.041 μH	442.9 μH	7.651 μH
L_2	29.27 μH	0.991 μH	453.5 μH	7.684 μH
L_3	28.88 μH	1.002 μH	447.3 μH	7.684 μH
L_4	28.81 μH	0.980 μH	446.5 μH	7.886 μH

UGC Approved Journal

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 4, Issue 8, August 2017

VII. CONCLUSION

This paper proposes a novel dc–dc converter topology to achieve an ultrahigh step-up ratio while maintaining a high conversion efficiency. It adopts a three degree of freedom approach in the circuit design. This paper has presented an ultrahigh step-up dc–dc topology based on a 3DoF topology. Through theoretical analysis and experimental tests, the proposed converter is proven to be advantageous. 1) A 3DoF design is achieved to improve the converter performance. The electrical isolation and modular structure of high step-up power cells are combined to increase the output voltage. 2) The voltage stress on primary switching devices of the coupled inductors is limited and soft switching of primary side switches is achieved. The proposed 3DoF converter can use low-voltage power devices to generate a high output voltage. In addition, the reverse-recovery issue with secondary rectifier diodes is also alleviated. 3) The two-section output voltage control and module idle control are developed to improve the controllability of the output voltage and converter efficiency over a wide power range. The developed techniques can be applied widely to high-voltage and high-power dc systems. By using the simulation results we can analyze the proposed method.

REFERENCES

[1] K. I. Hwu and Y. T. Yau, "High step-up converter based on coupling inductor and bootstrap capacitors with active clamping," IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2655–2660, Jun. 2014.

[2] Y. Gu, X. Xin, W. Li, and X. He, "Mode-adaptive decentralized control for renewable DC microgrid with enhanced reliability and flexibility,"IEEE Trans. Power Electron., vol. 29, no. 9, pp. 5072–5080, Sep. 2014.

[3] Y. Park, B. Jung, and S. Choi, "Nonisolated ZVZCS resonant PWM DCDC converter for high step-up and high-power applications,"IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3568–3575, Aug. 2012.

[4] W. Li, W. Li, X. Xiang, Y. Hu, and X. He, "High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications,"IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2829–2836, Jun. 2014.

[5] F. Evran and M. T. Aydemir, "Isolated high step-up DC-DC converter with low voltage stress,"IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3591–3603, Jul. 2014.

[6] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high efficiency fuel-cell power-generation system with active-clamp flyback– forward converter,"IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 599–610, Jan. 2012.

[7] W. Li and X. He, "Review of non-isolated high step-up DC/DC converters in photovoltaic grid-connected applications,"IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[8] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A safety enhanced, high step-up dc–dc converter for ac photovoltaic module application," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1809–1817, Apr. 2012.

[9] G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier,"IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3205–3214, Nov. 2011. [10] K. J. Lee, B. G. Park, R. Y. Kim, and D. S. Hyun, "Nonisolated ZVT twoinductor boost converter with a single resonant inductor for high step-up applications,